CLAIMS

1. A semiconductor capacitor having a first semiconductor layer which forms a first capacitor electrode (1) and which includes silicon, a second capacitor electrode (3) and a capacitor dielectric (5) including praseodymium oxide between the capacitor electrodes (2, 3),

characterised in that

provided between the capacitor dielectric (5) including praseodymium oxide and at least the first semiconductor layer (1) including silicon is a first thin intermediate layer (9) representing a diffusion barrier for oxygen.

2. A semiconductor capacitor as set forth in claim 1 characterised in that the first thin intermediate layer (9) includes oxynitride or titanium.

3. A semiconductor capacitor as set forth in claim 1 or claim 2 wherein the thickness of the first thin intermediate layer (9) is 0.5 nm or less.

4. A semiconductor capacitor as set forth in one of claims 1 through 3 wherein the second capacitor electrode (3) is formed from a second semiconductor layer and there is a second thin intermediate layer (11) between the second semiconductor layer and the capacitor dielectric (5) which includes praseodymium.

5. A semiconductor capacitor as set forth in claim 4 wherein the second thin intermediate layer (11) includes oxynitride.

6. A semiconductor capacitor as set forth in one of claims 4 wherein the second thin intermediate layer (11) includes silicon oxide.

7. A semiconductor capacitor as set forth in one of claims 4 through 6 wherein the thickness of the second thin intermediate layer (11) is 0.5 nm or less.

8. A semiconductor capacitor as set forth in claim 2 or claim 5 wherein the oxynitride of the first or the second thin intermediate layer (9, 11) has a concentration ratio of oxygen to nitrogen of 1:1.

9. A memory cell for a dynamic random access memory, which includes a semiconductor capacitor as set forth in one of claims 1 through 8.

10. A field effect transistor comprising a substrate (1), a gate oxide layer (5) and a gate electrode (3), which includes a semiconductor capacitor as set forth in one of claims 1 through 8, wherein the substrate (1) forms the first capacitor electrode, the gate electrode (3) forms the second capacitor electrode and the gate oxide (5) forms the capacitor dielectric.